22 11-16
84. The method of any one of claims ~~73-78~~, wherein data files are written to the flash EEprom system by writing to one or more blocks of EEprom cells, wherein the cells of each block are erasable together.

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~~85~~. The method of claim ~~84~~, wherein the flash EEprom system operates to map an address of a defective block of cells into another block of cells.

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~~86~~. The method of claim ~~84~~, wherein the flash EEprom system operates to erase the EEprom cells in multiple designated blocks at one time.

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25 11-16
~~87~~. The method of any one of claims ~~73-78~~, wherein writing a new data file to the cache memory from the host occurs in less time than if written directly into the flash EEprom memory from the host.

26 25
~~88~~. The method of claim ~~87~~, wherein writing the selected data file to the flash EEprom system includes programming individual memory cells of the flash EEprom system into more than two states in order to store more than one bit of data per cell.

## REMARKS

Claims 68-72, not acted upon by the Office Action, were added to the present application by a Second Preliminary Amendment that was filed February 17, 1998, over 3 months prior to the May 20, 1998 mailing date of the Office Action. This has already been pointed out in a Request for Supplementary Action, mailed to the Patent Office on May 28, 1998, which included a copy of the Amendment that was not considered as well as a copy of an Information Disclosure Statement that is not indicated in the Office Action to have been considered. The Information Disclosure Statement was also filed February 17, 1998, with copies of the references included in three 3-ring binders. Copies of these previously filed papers not yet considered are being filed herewith, except for copies of the references. An additional set of the references can be supplied by the undersigned, if they are not now available to the Examiner, in response to a telephone call to the undersigned attorney.

In a telephone conversation with Examiner Chung, initiated by the undersigned on September 25, 1998, it was indicated that the present application is not on her docket for action. She suggested that it was, therefore, necessary to respond to the outstanding Office Action, even though pending claims 68-72 had not yet been examined. No response to the undersigned's Request for

Supplementary Action is apparently going to be made. It is expected, however, that Applicants will not be prejudiced by the Patent Office's failure to consider the new claims and Information Disclosure Statement filed more than 3 months before the current Office Action was mailed.

Those of claims 63-72 that were examined, namely claims 63-67, stand rejected under 35 U.S.C. 103 over a single reference, U.S. patent no. 4,530,055 to Hamstra et al. (1985). That reference describes the use of a read cache memory in a disk drive memory system. The purpose of that cache is to store frequently read data files from the disk memory since data may be read more quickly from semiconductor memory which forms the cache than from the disk. That is the traditional roll of cache memories. A data file from the host is written directly to disk, and copies of frequently accessed files are maintained in the cache. Access to the frequently read data files is then had from the cache, thereby to improve the speed with which they may be read.

The Hamstra et al. patent also describes writing to the cache when the host system directs updating a file already stored in the cache, and then describes techniques of transferring that update to the copy of the data file stored on the disk. But any new data file written to the memory system from the host is written to the disk, and a copy is maintained in the cache only after it obtains a history of being frequently read. Any data file in cache is read from the cache and not from the disk. It is the purpose of a *read* cache in disk memory systems to read as much data from the cache as practical since the read speed is so much faster from the cache than from the disk. The Hamstra et al. patent reference uses its cache in this traditional way.

The present invention, on the other hand, is directed to the use of a *write* cache as part of a flash EEprom system. A new data file directed by the host computing system for storage in a mass storage system is first written to the cache memory and not written at that time to the flash EEprom system. This data file is then later written from the cache memory to the flash EEprom system when necessary, for example, to make room for other data files after the cache memory has become full. Once a data file is written into the flash EEprom system from the cache, it is read from the flash EEprom system. No copy of a data file need be kept in the cache to increase read speed, as is done by including a read cache in disk drives. These are the differences between the *write* cache being claimed and the typical disk drive *read* cache of the cited Hamstra et al. patent reference.

There are two reasons given in the present application for using a write cache with a flash EEprom system. First, flash EEprom cells change their characteristics after a large number of

cycles of being erased and re-programmed, and even have a maximum number of cycles that are practical. By storing and using new data files in the cache memory, the number of erase and programming cycles of the flash EEprom cells is reduced. A second reason for using a cache is that it can be faster to write a data file to the cache than to flash EEprom.

Each of the rejected claims 63 and 64 and unexamined claims 68 and 69, calls for writing new data files into the cache memory instead of the flash EEprom memory. This is not suggested by Hamstra et al. Indeed, it appears to be contrary to the way that the cited Hamstra et al. system operates. Hamstra et al. appear to write a data file directly to the cache memory only when updating a file that is also stored on disk but happens to reside in cache because it is frequently being accessed for read. As is typical for disk read cache, a new data file is first written to disk and then a copy written into cache if that data file is being frequently read.

Each of the rejected claims 65-67 and unexamined claims 70-72, now recites, in its last paragraph being added by this Amendment, that data files are read from the flash EEprom system rather than from the cache memory. This is completely contrary to a typical disk storage system read cache of the type described by Hamstra et al., wherein as many files as possible reside in the cache so that they may be read more quickly than is possible by accessing the disk memory.

Further, there is no suggestion by Hamstra et al. of using a cache memory that may be cycled significantly more that the primary memory (disk in Hamstra et al., and flash EEprom in the present claims), as recited in each of the rejected claims 63-67. Nor does Hamstra et al. discuss using a cache memory because it is faster to write to the cache than to its primary disk memory. Thus, neither of the motivations for the present invention that are discussed in the present application for using a *write* cache memory exist in a disk system with a *read* cache of the cited reference.

Indeed, the broad idea, included in all the claims, of using a write cache with a flash EEprom system would not have been obvious. The Office Action, without citing any reference, takes Official Notice of the alleged fact that it would have been obvious to substitute the claimed flash EEprom system for the disk system of Hamstra et al. If the present rejection is maintained, citation of evidence of this assumed fact is requested. Cache memories have long been used to overcome the relatively slow speed at which disk systems can be read. This is not the motivation for using a cache memory in the present invention, as discussed in the preceding paragraph. There has been no showing that it would have been obvious, on or before the April 13, 1989 effective filing date of the

present application, to combine any type of cache with a flash EEprom system, let alone the specific *write* cache being claimed. It seems more likely that one ordinarily skilled in the art would have thought that the use of a semiconductor flash EEprom system as the mass storage memory eliminated the need for another semiconductor memory in the form of a cache.

Each of the unexamined claims 68-72 also recites that the flash EEprom system is programmable into more than two states in order to store more than one bit per memory cell. It would particularly not have been expected to use a cache memory, which normally was ordinary two-state dynamic random access memory (DRAM), with a multi-state flash EEprom system. A data file is effectively compressed when it is read from a certain number of cells of a two state cache and then written into only one-half that number of flash EEprom cells operated in four states. Even fewer flash EEprom cells are required if the cells individually have more than four storage states.

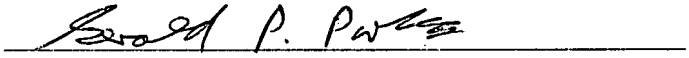
Only one independent claim is being added by this Amendment, namely claim 73. In addition to defining the basic non-obvious use of a write cache with a flash EEprom system, this claim includes two other novel operating features discussed above with respect to others of the claims. One is that all new data files from the host are written to the cache memory without writing them to the flash EEprom system. The other specific feature is that data files are read from the flash EEprom system and not the cache memory. Claim 73 is thus clearly allowable.

New dependent claims 74-88 add additional novel features to the data storage method of claim 73. For example, claims 81, 83 and 88 recite the multi-state flash EEprom operation, as discussed above with respect to claims 68-72. Claims 87 and 88 include the feature of writing faster to cache than to the flash EEprom, which is the reverse for the prior art cache used with a disk drive. Claims 84-86 recite specific novel flash EEprom operating features.

Accordingly, an early indication of the allowance of this application is solicited.

Dated: October 6, 1998

Respectfully submitted,



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